Jonah Pflaster

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Education

Tufts University, Medford, MA *Expected May 2027 | GPA: 3.8*
B.S. Computer Engineering | Minor in Mathematics

Experience

Watershed Ventures, AI Software Engineering Intern *New York, NY (Hybrid)*
May 2025 – Present

- Designed and shipped a production multi-agent intelligence platform that sources and scores **thousands of companies per day** and generates memos for **tens to hundreds of companies per month**
- Deployed and operated on **AWS EC2** with **PostgreSQL** and a **Next.js** internal dashboard; emphasized reliability, observability, and performance under continuous workloads
- Built structured pipelines for enrichment and evaluation with validation and retries to improve consistency and debuggability
- *Tech:* Python, TypeScript, Next.js, PostgreSQL, Supabase, AWS

Tufts University, Teaching Assistant, CS 11 *Medford, MA*
Sep 2025 – Present

- Lead lab sections and office hours; support 100+ students through debugging, testing habits, and core programming fundamentals
- Grade assignments and exams with feedback on correctness, code style, and edge-case handling

Engineers Without Borders, Technical Lead *Medford, MA*
Aug 2024 – May 2025

- Led a 10–20 member subteam building a real-time water catchment monitoring system, including sensing, calibration, and failure detection logic
- Prototyped Arduino-based measurement pipelines and documented repeatable calibration and deployment procedures for field use
- Integrated hardware-to-reporting workflow emphasizing reliability in constrained environments

SoundSense, LLC, Engineering Intern *Wainscott, NY*
Jun 2024 – Aug 2024

- Performed measurement-driven data analysis for acoustical engineering field studies and contributed calculations used in client deliverables
- Supported modeling and reporting workflows using Excel, QuickBase, and SketchUp

Selected Projects

LEGv8 64-bit ARM CPU *Project Page*
VHDL, ARM LEGv8 ISA, GHDL, GTKWave

- Implemented a 64-bit LEGv8 CPU progressing from single-cycle to a 5-stage pipelined architecture
- Built forwarding and hazard detection logic to resolve pipeline dependencies and reduce stalls
- Verified correctness via cycle-accurate simulation in GHDL and waveform-level debugging in GTKWave

Smoosh Bros (FPGA Fighting Game) *Project Page*
SystemVerilog, FPGA, VGA, Controllers

- Built a two-player fighting game fully in hardware on an iCE40UP5K FPGA with VGA 640x480 output and NES controller input
- Implemented sprite rendering, collision detection, and game state logic; validated timing and on-board behavior through testing

HandJam *Project Page*
Python, TensorFlow, Embedded ML, STM32

- Deployed real-time computer vision inference on an STM32 NUCLEO-L432KC for gesture recognition and interactive audio control
- Trained on 2000 labeled images; achieved 90–100% accuracy in controlled conditions

Technical Skills

Languages: C, C++, Python, VHDL, SystemVerilog
Hardware/Embedded: Microcontrollers, GPIO, timers, interrupts, Arduino, STM32, Raspberry Pi, FPGA, CAD
Tools/Systems: Git, Linux, GHDL, GTKWave, AWS, PostgreSQL